10 GHz-10 W INTERNALLY MATCHED FLIP-CHIP GaAs POWER FETS

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ABSTRACT

The flip-chip GaAs power f.e.t. delivering 10 W power output with 3 dB gain has been realized at 10 GHz by using a newly developed internal matching technique, in which the f.e.t. chips are directly connected to the lumped dielectric capacitors prepared for the matching networks.

Introduction

Recently, GaAs power m.e.s.f.e.t.s with various configurations have been developed at a number of laboratories.[1] Above all, the structure with the flip-chip mounting for all three terminals is favourable in obtaining superior r.f. performance above X-band frequencies because of small parasitic inductances and good heat dissipation.[2] However, it has been pointed out that the fabrication of the internally matched flip-chip power f.e.t.s is difficult above X-band frequencies because of large electric distance from the gate electrodes to the input lumped matching network.[1]

We have overcome this problem by developing a new type of the internally matching configuration, in which gold plated gate and drain metal posts are directly connected to the electrodes of the dielectric capacitors.

This paper describes a newly developed configuration of the internally matched flip-chip GaAs power f.e.t. and the microwave performance.

Device Structure

Figure 1 shows a scanning-electron microphotograph of the f.e.t. chips used in this work. The single chip is composed of three unit cells, each of which has twelve gate fingers 200 μm wide and 1 μm long. Source-to-gate and source-to-drain spacings are 1.5 μm and 4 μm, respectively. Total gate width of the chip is 7200 μm. Gold is electroplated on the source, drain and gate pads as thick as 20-30 μm. The metal layers of titanium, platinum and gold are formed between the gold post and the aluminum gate pad to prevent aluminum-gold interaction.

Figure 2(a) and 2(b) show the top and cross sectional views of an internally matched 4-chips device (W_{gt} = 28800 μm) mounted on a chip carrier. The chip carrier, which is 8.0 mm long and 5.0 mm wide, consists of the chip mount, the input and output impedance matching networks and the 50 ohm microstrip lines. Both the input and output matching networks are composed of two lumped shunt capacitors and lumped series inductors. The lumped capacitors were formed on the dielectric substrates (relative dielectric constant of 41) with the thickness of 0.4 mm, which were leveled with the source heat sink. The f.e.t. chip is turned over and the gate and drain metal posts are directly connected by thermocompression bonding to the electrodes of the dielectric capacitors prepared for the input and output matching networks. The source metal posts are also directly bonded to the gold plated copper heat sink. The pressure of thermocompression bonding is less than 180 kg/cm^2 at 350°C, which gives no serious damage to the device. This configuration gives extremely reduced electric distance from the gate electrodes to the lumped capacitors. Therefore, it becomes easily possible to increase the center frequency of the lumped matching networks up to frequencies above X-band.

Both the input and output impedance matching are realized by adjusting the chip capacitances C and the wire inductances L of the lumped L-C circuits. The circuit design procedure was based on the small signal S parameters of the chip with appropriate modification of the output lumped L and C taking the large signal effects into account.[3] In this study, the center frequency of the lumped matching network was adjusted mainly to 10 GHz.

Performance

Typical power output versus power input curves at 10 GHz for 1-chip (W_{gt} = 7200 μm), 2-chips (14400 μm) and 4-chips (28800 μm) devices are shown in Fig. 3 together with the power added efficiencies. Most devices are operated at a drain voltage of 10 to 11 V and a gate voltage of -0.5 to -1.5 V. A 4-chips device gives power output of 10 W with 3.0 dB gain and power added efficiency of 14 %. A 1-chip device gives the 1 dB gain compression of 3.4 W with linear power gain as high as 8.0 dB at 10 GHz. Figure 4 shows the power output at 1 dB gain compression and the linear power gain versus the total gate width. It is noted that no sudden decrease in a power combining efficiency and the linear power gain is observed up to the total gate width of 28800 μm. Figure 5 shows the frequency response of the 4-chips and 1-chip internally matched

flip-chip f.e.t.s. The 4-chips device covers the 9.5-10.3 GHz frequency range with ± 0.5 dB gain ripple. When the center frequency of a 1-chip device was adjusted to 11 GHz and 12 GHz, the typical input-output characteristics shown in Fig.6 were obtained. The 1-chip device gives the 1 dB gain compression of 3.0 W with the linear power gain of 5.3 dB at 12 GHz. The best results obtained are presented in Table I.

Conclusion

10 W at 10 GHz was realized with a newly developed internal matching configuration of the flip-chip GaAs power f.e.t., in which the gate and drain electrodes were directly connected to the lumped matching capacitors with no bonding wires. The result implies that this configuration is favourable in obtaining power f.e.t.s with sufficient gain and power output at the X band frequency.

Acknowledgement

The authors wish to thank Dr. K. Shirahata for his encouragement throughout this work.

References

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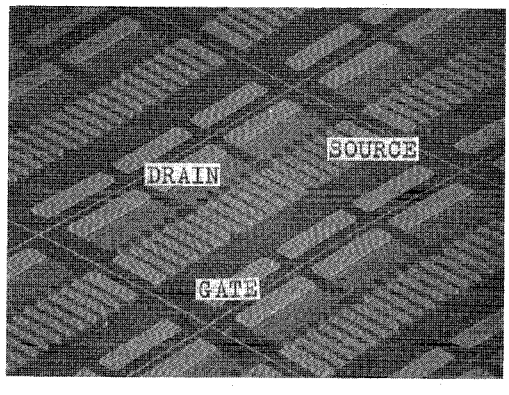
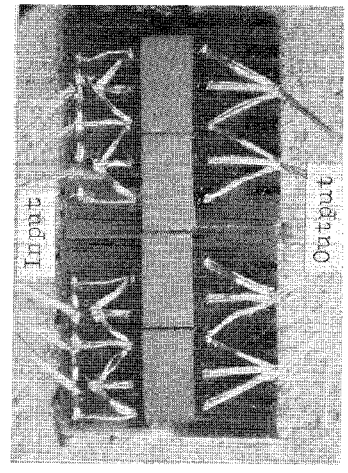
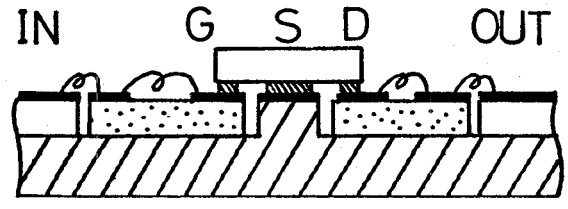


Fig. 1 Scanning electron microphotograph of the f.e.t. chips



2(a)



2(b)

Fig. 2 Top view (Fig. 2(a)) and cross sectional view (Fig. 2(b)) of an internally matched 4-chips device (W_{gt} = 28800 μm)

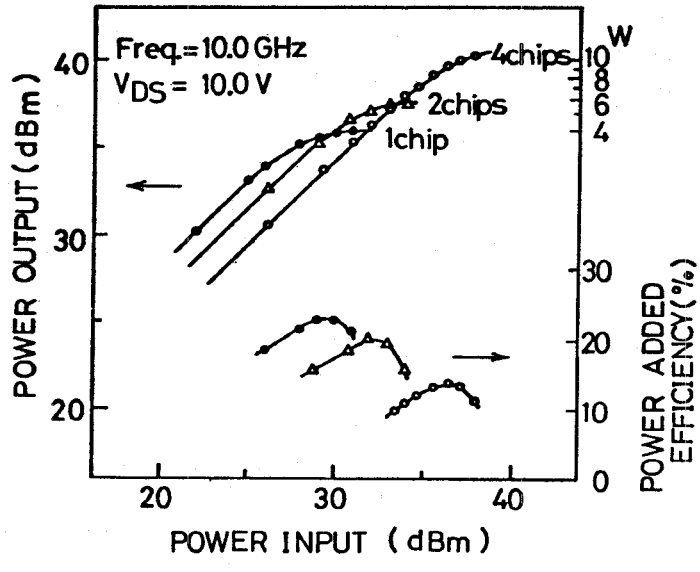


Fig. 3 Power output and power added efficiency versus power input curves for the 1-chip (W_{gt} = 7200 μm), 2-chips (14400 μm), and 4-chips (28800 μm) devices at 10 GHz

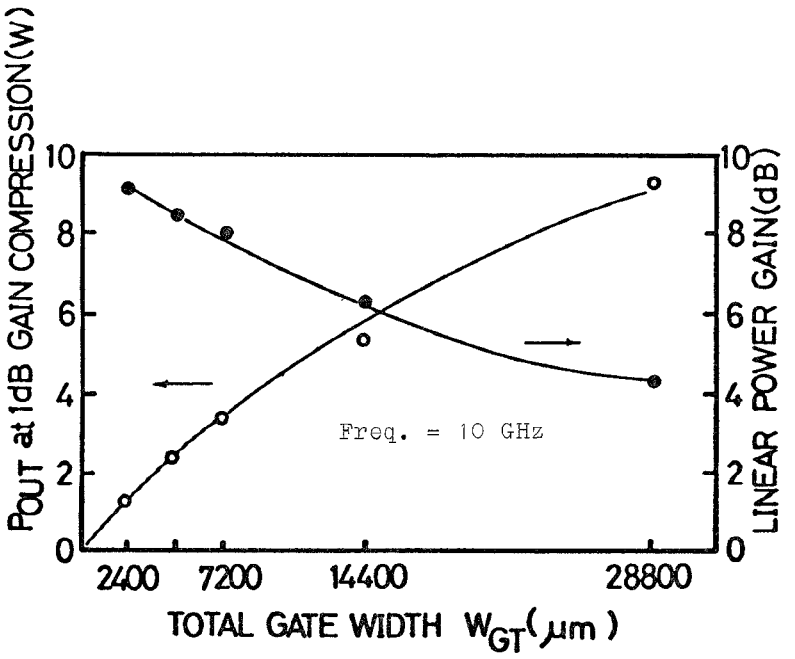


Fig. 4 Power output at 1 dB gain compression and linear power gain at 10 GHz against total gate width

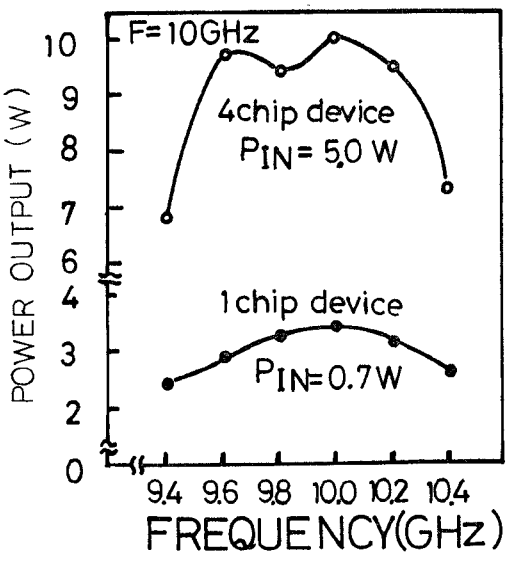


Fig. 5 Frequency response of the 4-chips and 1-chip internally matched flip-chip f.e.t.s.

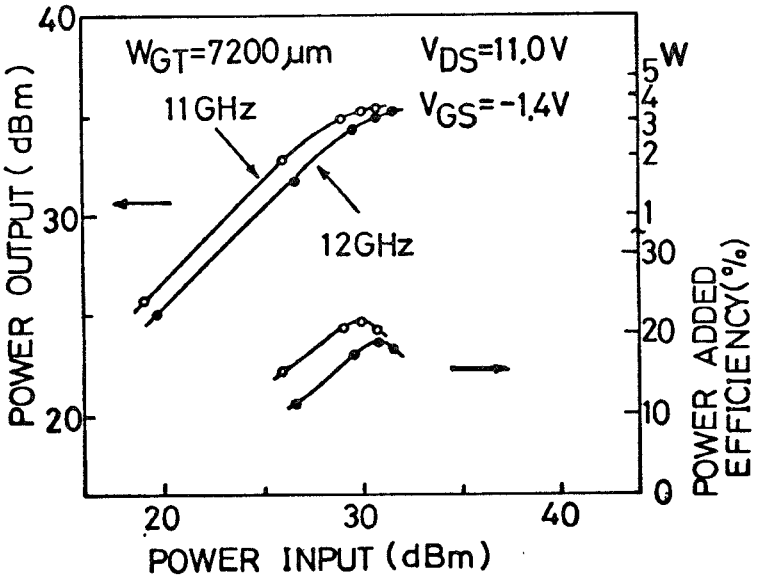


Fig. 6 Power output versus power input curves at 11 GHz and 12 GHz for the 1-chip device

Table. I Internally matched GaAs flip-chip power FET performance

f(GHz)	P_{SAT}(W)	P_{1dB}(W)	G_{LP}(dB)	η_{add}(%)	W_{GT}(μm)
10.0	11.5	9.3	4.3	14	28800
10.0	5.8	5.3	6.3	20	14400
10.0	4.0	3.4	8.0	23	7200
10.0	2.6	2.4	8.4	28	4800
12.0	3.5	3.0	5.3	19	7200